IN THE CLAIMS:

Please cancel claims 1-15 without prejudice or disclaimer. Applicant reserves the right to reintroduce any of the claims, if necessary, at a later date.

Please amend the claims as follows:

Amendments to the Claims

This listing will replace all prior versions and listings of claims in the application:

Listing of Claims

Claims 1-15 (canceled)

16. (currently amended) A microjoint interconnect structure comprising:

(a) a carrier substrate having an array of interconnects for connecting device components; said

~~(b) the~~ carrier, including a substrate and a dielectric film, and microjoint receptacles comprising an adhesion layer, diffusion barrier layer and a noble metal layer.; and

(~~c~~b) microjoining pads on the device side, comprising an adhesion layer, solder reaction barrier layer and fusible solder joint ball for each component;

~~(d)~~ said microjoint pads on the device on the carrier side matching said microjoint receptacles on the carrier side.

17. (currently amended) A microjoint interconnect structure as defined in Claim 16 wherein the device components are selected from the group consisting of: semiconductor chips and, optical component chips ~~and the like~~.

18. (currently amended) A process for connecting a set of device chips by means of an array of microjoint structures on an interconnect carrier, said process comprising:

forming the carrier including a multilayer substrate having a plurality of microjoint receptacles in one surface;~~.~~

forming a set of microjoint pads, including solder balls, on the device chips joined to the receptacles in the one carrier surface~~,~~; and

forming interconnect wiring mounted in the carrier connecting to the microjoint pad arrays to enable the interconnection between device chips mounted on the carrier.

19. (currently amended) A microjoint interconnect structure comprising:

(a) a carrier substrate having an array of interconnects for connecting device components~~.~~;

~~(b)~~ the carrier, including a substrate and dielectric film with microjoining pads each comprising an adhesion layer, solder reaction barrier layers and fusible solder joint ball~~.~~; and

(~~c~~b) ~~the~~ microjoint receptacles on the device side comprising an adhesion layer, diffusion barrier layer and a noble metal layer~~.~~;

~~(d)~~ said microjoint pads on the carrier side matching said microjoint receptacles on the device.

20. (currently amended) A microjoint interconnect structure as defined in Claim 19 wherein the device chips are selected from the group ~~comprising~~

consisting of: semiconductor chips, optical device chips, and communication chips.

21. (currently amended) A process for connecting a set of device chips by means of an array of microjoint structures on an interconnect carrier, said process comprising:

forming the carrier including a multilayer substrate having a plurality of microjoint pads including solder balls on one surface;

forming a set of microjoint receptacles on one surface of the device chips that are joined to the carrier by the solder balls on the carrier; and

forming interconnect wiring on the carrier connecting the microjoint pad arrays to enable the interconnection between the chips.

22. (new) The process of Claim 19, wherein said receptacles on said interconnect carrier comprise successive layers of a liner layer, seed layer, barrier layer and a noble metal layer, respectively, these layers lining the inner surface of said receptacles.

23 (new) The process of Claim 22, wherein the liner layer is selected from the group consisting of Ta, TaN, Ti, TiN, W, WN, Cr and combination thereof.

24. (new) The process of Claim 23, wherein the liner layer thickness is between 50Å and 1200Å.

25. (new) The process of Claim 22, wherein the seed layer is copper with thickness in the range 300Å to 2000Å.

26. (new) The process of Claim 22, wherein the barrier layer is selected from the group consisting of Ni, Co, Pt, Pd and alloys or combinations thereof.

27. (new) The process of Claim 26 wherein the barrier layer thickness is between 1000Å and 10,000Å.

28. (new) The process of Claim 19 wherein said microjoint pads on said device chips comprise successive layers of a liner layer, seed layer, barrier layer and a fusible solder layer, respectively.

29. (new) The process of Claim 28 wherein the liner layer is selected from the group comprising Ta, TaN, Ti, TiN, W, WN, Cr and combinations thereof.

30. (new) The process of Claim 28 wherein the seed layer is copper with thickness in the range 300Å to 2000Å.

31. (new) The process of Claim 28 wherein the barrier layer is selected from the group comprising Ni, Co, Pt, Pd and alloys or combinations thereof.

32. (new) The process of Claim 31 wherein the barrier layer thickness is between 1000Å and 10,000Å.

33. (new) The process of Claim 22 wherein the carrier is made of silicon and includes a set of interconnect wiring disposed thereon, a dielectric passivation layer over the top surface of the interconnect wiring and said receptacles being in the dielectric passivation layer.

34. (new) The process of Claim 32 wherein the device chiplet includes a set of devices built on it connected by wiring, a dielectric passivation layer over the top surface of the wiring and said microjoint pads being in the dielectric passivation layer.

35. (new) The process of Claim 32 wherein the device chiplets are selected from the group comprising microprocessor chip, memory chip, microcontroller chip, laser diode chip, laser driver chip, photodetector chip, wireless communication chip, and logic processor chip.